Application No. 09/591,044
Filed: June 9, 2000
Group Art Unit: 2189

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended): A system for transferring data between a plurality of devices, comprising:

a bus including at least one data line for transmitting the data and at least one clock line; and

~~a~~ at least one first device communicably coupled to the bus~~,~~ , ~~and~~

~~a second device communicably coupled to the bus,~~

wherein the ~~system~~ first device is operative at a first clock rate and at a second reduced clock rate, the reduced clock rate being less than the first clock rate, and

wherein the first device is operative ~~at least at the second clock rate~~ to receive at least a portion of the data transmitted over the data line, and to store the at least a portion of the data in a register, and

~~wherein the second device is operative at least at the second clock rate~~in the event the first device is operating at the reduced clock rate, to drive the clock line to a ~~low~~ first predetermined logic level while the data is stored in the register, thereby enabling data transfer between ~~of~~ the first device and at least one second device over the bus while the first device operates at the reduced clock rate.

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Claim 2 (Currently amended): The system of claim 1 wherein the first device is further operative at least at the second clock rate to clear the data from the register upon completion of ~~a~~ the data transfer.

Claim 3 (Currently amended): The system of claim 1 further including pull-up circuitry for pulling the clock line to a ~~high~~ second predetermined logic level, and wherein the ~~second~~ first device is further operative to release the clock line upon completion of ~~a~~the data transfer to allow the clock line to be pulled ~~high~~ to the second predetermined logic level by the pull-up circuitry.

Claim 4 (Currently amended): The system of claim 1 further including pull-up circuitry for pulling the clock line to a ~~high~~ second predetermined logic level, and wherein, upon completion of ~~a~~the data transfer, the first device is further operative to clear the data from the register, and ~~the second device is further operative~~ to release the clock line to allow the clock line to be pulled ~~high~~ to the second predetermined logic level by the pull-up circuitry.

Claim 5 (Original): The system of claim 1 wherein the bus comprises an SMBus.

Claim 6 (Currently amended): A method of transferring data between a plurality of devices, comprising the steps of:

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storing at least a portion of the data in a register by at least one first device communicably coupled to a bus, the bus including at least one data line for transmitting the data~~,~~ and at least one clock line ~~for transmitting a clock signal~~, the first device being operative at a first clock rate and at a second reduced clock rate, the reduce clock rate being less than the first clock rate~~, the storing step including storing the at least a portion of the data in the register while the clock signal is being transmitted at least at the second clock rate~~; and

in the event the first device is operating at the reduced clock rate, driving the clock line to a ~~low~~ first predetermined logic level while the data is stored in the register by the first device, thereby enabling data transfer between the first device and at least one second device over the bus while the first device operates at the reduced clock rate.

Claim 7 (Currently amended): The method of claim 6 further including the step of clearing the data from the register upon completion of ~~a~~the data transfer by the first device.

Claim 8 (Currently amended): The method of claim 6 wherein the clock line is pulled to a ~~high~~ second predetermined logic level by pull-up circuitry, and further including the step of releasing the clock line upon completion of ~~a~~the data transfer by the first

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device, ~~to allow~~ thereby allowing the clock line to be pulled ~~high~~ to the second predetermined logic level by the pull-up circuitry.

Claim 9 (Currently amended): The method of claim 6 wherein the clock line is pulled to a ~~high~~ second predetermined logic level by pull-up circuitry, and further including the steps of, upon completion of ~~a~~the data transfer, clearing the data from the register and releasing the clock line by the first device, thereby ~~to allow~~ allowing the clock line to be pulled ~~high~~ to the second predetermined logic level by the pull-up circuitry.

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